REMARKS

Claims 1-13 and 16-24 are pending, with claims 1, 9, 16, and 21 being independent. In response to a restriction requirement communicated by telephone, Group II, claims 9-13 and 21-24, has been elected without traverse. Claims of Group I, claims 1-8 and 16-20, are withdrawn from consideration.

The indication of allowable subject matter in claims 22-23 is acknowledged and appreciated.

Claims 9-13, 21 and 24 stand rejected under 35 U.S.C. 102(a) as allegedly being anticipated by Nakai et al. (US Patent 6,115,728). This contention is respectfully traversed.

Independent claim 9 is patentable over Nakai because Nakai fails to teach or suggest all of the elements of claim 9. Claim 9 includes control and address generation circuitry comprising "a second memory which stores pre-programmed processing and control data". The official action suggests that RAM#1 (item 102 in FIG. 1) of Nakai meets this limitation. However, as clearly illustrated in FIG. 1, RAM#1 is not included in the RAM Address Generator 105 in Nakai, which the official action identifies as the control and address generation circuitry. Thus, this element of claim 9 is not taught by Nakai.

Moreover, RAM#1 in Nakai stores "input/output data and intermediate data obtained during a butterfly operation". (See

Nakai at col. 8, lines 30-33.) Nowhere does Nakai suggest that RAM#1 stores pre-programmed processing and control data, as claimed. For this additional reason, the second memory of claim 9 is not taught by Nakai.

Furthermore, the multiplexer structures of claim 9 are nowhere suggested in Nakai. The claimed control and address generation circuitry comprises "a first set of multiplexers, each of which having at least one direct input for receiving transformation data, and another input, into which said transformation data is fed via a corresponding inverter, said first set being controlled to transfer transformation data or, inverted transformation data, by a predetermined value provided by said transformation data".

The official action identifies the multiplexers 121 in Nakai as corresponding to the first set of claimed multiplexers. But FIG. 1 clearly shows that the multiplexers 121 in Nakai are not included in the RAM Address Generator 105, which the official action identifies as the control and address generation circuitry.

Moreover, the inputs of the multiplexers 121 in Nakai are a data input and an output from the butterfly operation unit 103. Nowhere does Nakai teach a set of multiplexers that each have at least one direct input for receiving transformation data, and

another input, into which said transformation data is fed via a corresponding inverter.

Additionally, nowhere in Nakai is there a suggestion that a set of multiplexers can be controlled to transfer transformation data or, inverted transformation data, by a predetermined value provided by said transformation data. For all of these reasons, the claimed first set of multiplexers is not taught by Nakai.

The control and address generation circuitry of claim 9 also comprises "a second set of multiplexers, each of which having at least one input connected to the output of a corresponding multiplexer selected from said first set of multiplexers, and another input, connected to said second memory, said second set being controlled by said comparator circuitry to provide a first address to the first memory by transferring the output of each multiplexer from said first set to the output of its corresponding multiplexer from said second set or, to provide at least a portion of the second address to the first memory by transferring data stored in said second memory".

The official action identifies the multiplexers 122 in Nakai as corresponding to the second set of claimed multiplexers. But again, FIG. 1 clearly shows that the

multiplexers 122 in Nakai are not included in the RAM Address Generator 105.

Moreover, the inputs of the multiplexers 122 in Nakai are the outputs of the two RAMs #0 and #1. Nowhere does Nakai suggest that an input of a multiplexer in the set 122 could be connected to an output of a corresponding multiplexer from the set 121, as would be required by the interpretation of claim 9 presented in the official action.

Similarly, Nakai fails to teach or suggest that the multiplexers 122 can be controlled to provide a first address to the first memory by transferring the output of each multiplexer from said first set to the output of its corresponding multiplexer from said second set or, to provide at least a portion of the second address to the first memory by transferring data stored in said second memory. For all of these reasons, the claimed second set of multiplexers is not taught by Nakai.

Finally, the control and address generation circuitry of claim 9 also comprises "a multiplexer, operating in combination with said second set of multiplexers in said data processing mode, having an unconnected input and an input connected to said second memory and controlled by said comparator circuitry, thereby providing the remaining portion of said second

address". The official action identifies the same set of multiplexers 122 as being this third multiplexer that operates in combination with the second set of multiplexers 122 in Nakai.

Assuming for the sake of argument that the two multiplexers 122 in Nakai can be both a set of multiplexers and a multiplexer operating in combination with the set of multiplexers, Nakai still does not teach or suggest the claimed element. In particular, the multiplexers 122 do not have an unconnected input, as claimed, nor do they provide an address or a portion of an address to a memory.

For all of these reasons, independent claim 9 should be allowable. Dependent claims 10-13 are patentable based on the above arguments and their own merits.

With respect to independent claim 21, the official action states that this claim is rejected under the same rationale as claim 12, since claim 21 has "similar limitation". While it is true that claim 21 is similar to claim 12, claim 21 does in fact include different limitations and is of different scope. Independent claim 21 is patentable over Nakai because Nakai fails to teach or suggest all of the elements of claim 21.

Nakai fails to teach or suggest first and second inputs that receive input data and predetermined transformation data from means for reducing dimensions of and normalizing general

real and complex matrices corresponding to linear transformations. Nakai fails to teach or suggest transformation and accumulation circuitry that acts on the input data and the predetermined transformation data to produce an output vector of a linear transformation corresponding to the predetermined transformation data, wherein the transformation and accumulation circuitry comprises an adder and a memory.

Finally, Nakai fails to teach or suggest control and address generation circuitry, connected to the transformation and accumulation circuitry, wherein the control and address generation circuitry generates corresponding addresses for accessing cells of said memory, and for controlling selection between a data receiving mode, in which the input data is received via said first input and stored in the memory according to addresses corresponding to matrix columns, and a data processing mode, in which accumulating operations add or subtract data from one cell of the memory to another cell of the memory. Thus, independent claim 21 should be allowable. Dependent claim 24 is patentable based on the above arguments and its own merits.

It is respectfully suggested for all of these reasons, that the current rejection is totally overcome; that none of the cited art teaches or suggests the features which are now

claimed, and therefore that all of these claims should be in condition for allowance.

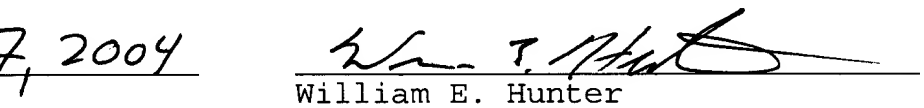
It is believed that all of the pending claims have been addressed. However, the absence of a reply to a specific issue or comment does not signify agreement with or concession of that issue or comment. Because the arguments made above may not be exhaustive, there may be reasons for patentability of any or all pending claims (or other claims) that have not been expressed. Finally, nothing in this paper should be construed as an intent to concede any issue with regard to any claim, except as specifically stated in this paper.

In view of the above, therefore, all of the claims should be in condition for allowance. A formal notice of allowance is thus respectfully requested.

No fees are believed due with this response. Please apply any necessary charges or credits to Deposit Account No. 06-1050.

Respectfully submitted,

Date: Sept. 17, 2004



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